CLAIMS

1. (Currently amended) A process for fabricating a semiconductor device having a ONO structure, comprising:

providing a semiconductor substrate;

forming on the semiconductor substrate an oxide layer;

depositing on the bottom oxide layer a nitride layer, the deposited nitride layer having a first hydrogen content; and

applying a treatment to reduce the first hydrogen content to a second hydrogen content, wherein the second hydrogen content is less than about two atomic percent.

2. (Original) The process of claim 1, wherein the treatment comprises one or more of RTO oxidation of at least a portion of the charge trapping dielectric charge storage layer in an oxidizing atmosphere, ISSG oxidation of at least a portion of the charge trapping dielectric charge storage layer, free radical oxidation of at least a portion of the charge trapping dielectric charge storage layer, decoupled plasma oxidation of at least a portion of the charge trapping dielectric charge storage layer, and steam oxidation of at least a portion of the charge trapping dielectric charge storage layer at a temperature in the range from about 400°C to about 1100°C.

3. (Original) The process of claim 1, wherein the first hydrogen content is in a range from greater than about 2 atomic percent to about 30 atomic percent.

4. (Currently amended) The process of claim 1, wherein the second hydrogen content is less than about ~~two~~ 0.1 atomic percent.

5. (Currently amended) The process of ~~claim 4~~ claim 1, wherein the second hydrogen content is in the range from about 0.1 atomic percent to about 0.5 atomic percent.

6. (Currently amended) The process of ~~claim 4~~ claim 1, wherein the second hydrogen content is substantially zero or not detectable by FTIR.

7. (Original) The process of claim 1, wherein hydrogen substantially does not migrate into the bottom oxide layer from the nitride layer during subsequent processing or in use.

8. (Original) The process of claim 1, further comprising forming on the nitride layer a top oxide layer by a method which does not impart hydrogen to the nitride layer.

9. (Original) The process of claim 8, wherein the top oxide layer is formed by one of oxidation of a portion of the nitride layer or deposition using low-hydrogen starting materials.

10. (Currently amended) A process for fabricating a charge trapping dielectric flash memory device comprising:

providing a semiconductor substrate;

forming on the semiconductor substrate a bottom oxide layer;

depositing on the bottom oxide layer a charge trapping dielectric charge storage layer, the deposited charge trapping dielectric charge storage layer having a first hydrogen content; and

applying a treatment to reduce the first hydrogen content to a second hydrogen content, wherein the second hydrogen content is less than about two atomic percent.

11. (Original) The process of claim 10, wherein the treatment comprises one or more of RTO oxidation of at least a portion of the charge trapping dielectric charge storage layer in an oxidizing atmosphere, ISSG oxidation of at least a portion of the charge trapping dielectric charge storage layer, free radical oxidation of at least a

portion of the charge trapping dielectric charge storage layer, decoupled plasma oxidation of at least a portion of the charge trapping dielectric charge storage layer, and steam oxidation of at least a portion of the charge trapping dielectric charge storage layer at a temperature in the range from about 400°C to about 1100°C.

12. (Original) The process of claim 10, wherein the first hydrogen content is in a range from greater than about 2 atomic percent to about 30 atomic percent.

13. (Currently amended) The process of claim 10, wherein the second hydrogen content is less than about ~~two~~ 0.1 atomic percent.

14. (Currently amended) The process of ~~claim 13~~ claim 10, wherein the second hydrogen content is in the range from about 0.1 atomic percent to about 0.5 atomic percent.

15. (Currently amended) The process of ~~claim 13~~ claim 10, wherein the second hydrogen content is substantially zero or not detectable by FTIR.

16. (Original) The process of claim 10, wherein hydrogen substantially does not migrate into the bottom oxide layer from the charge storage layer during subsequent processing or in use.

17. (Original) The process of claim 10, further comprising forming on the charge storage layer a top oxide layer by a method which does not impart hydrogen to the charge storage layer.

18. (Original) The process of claim 17, wherein the top oxide layer is formed by one of oxidation of a portion of the nitride layer or deposition using low-

hydrogen starting materials, wherein the low-hydrogen starting materials comprise one or more of TCS, DCS, BTBAS.

19. (Original) A charge trapping dielectric flash memory device comprising:

a semiconductor substrate having formed thereon a gate stack comprising a charge trapping dielectric charge storage layer; and

wherein the charge trapping dielectric charge storage layer comprises a hydrogen content less than about two atomic percent.

20. (Original) The device of claim 19, wherein the hydrogen content is in the range from about 0.1 atomic percent to about 0.5 atomic percent.